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EHF HETEROJUNCTION BIPOLAR TRANSISTORS

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16. Abstract (Limit 200 Words)

Progress has been made in the fabrication of InAlAs/InGaAs HBTs on both InP and GaAs substrates, high gain pnp HBTs, and the optimization of AlGaAs/InGaAs/GaAs HBTs for EHF applications. The first successful demonstration of InGaAs/AlGaAs HBT structures on GaAs substrates was made using MOCVD grown InP buffer layers. The performance of both S-HBT and D-HBT structures grown on InP and GaAs substrates was compared. A comprehensive mask set was designed and fabricated for millimeter-wave evaluation of HBTs.

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INTERIM TECHNICAL REPORT NO. 1
FOR
EHF HETEROJUNCTION BIPOLAR TRANSISTORS
CONTRACT NO. N00014-88-C-0613

I. SUMMARY OF PROGRAM GOALS

The aim of this program is development of a heterojunction bipolar transistor (HBT) for power generation and amplification at millimeter-wave frequencies. The device will be produced on a semi-insulating (SI) GaAs substrate for monolithic compatibility and will have InGaAs/InP(InAlAs) active layers. The development program will consist of nine tasks addressing the development of materials, processing, and device modeling.

Task 1 addresses the growth of EHF HBT structures on InP substrates to establish the optimum device structure on GaAs substrates. Task 2 addresses the growth of the optimum device structure. In Task 3, HBT structures are characterized to aid in materials development.

Tasks 4, 5, and 6 are the design and fabrication of initial HBT structures, process development, and performance optimization of devices based on InGaAs/InP(InAlAs) structures grown on GaAs substrates.

Task 7 is the development of complementary HBT structures. The optimized npn and pnp structures will be integrated on the same wafer under this task to produce complementary devices with higher output power and efficiency. Task 8 consists of millimeter-wave measurement and characterization to aid in device development. In Task 9, we will undertake comprehensive device modeling, also to aid in device development and optimization.

The program objective is fabrication and characterization of heterojunction bipolar transistors with the performance goals listed in Table 1.

Table 1. Performance Goals of Millimeter-Wave HBTs

Frequency (GHz)	Output Power (W)	Gain (dB)	Efficiency (%)
44	1	6	40
60	0.5	6	30
94	0.25	6	20

II. PROGRESS

To determine if strained layers can be used to enhance device performance for GaAs-based HBTs (Tasks 4 and 5), we have investigated the use of InGaAs layers in the base and emitter cap layer. The purpose is to aid in formation of ohmic contacts and, in the case of InGaAs in the base region, also to serve as an etch stop. Figure 1 shows the common-emitter characteristics of a large-area AlGaAs/GaAs HBT with a 100 Å $In_{0.1}Ga_{0.9}As$ etch-stop layer in the base. The current gain is about 100, and the base doping is 1×19 cm^{-3}. A device with 2-μm-wide and 20-μm-long emitter fingers exhibited a current gain cutoff frequency F_t of 35 GHz, and a maximum frequency of oscillation of 40 GHz. The performance of this device is comparable to that of a GaAs/AlGaAs control device with no InGaAs layers, so we conclude that the use of InGaAs contact layers does not significantly improve performance. However, the use of an InGaAs etch-stop layer in the base greatly simplifies device processing, which will enable us to use thinner base regions with reduced transit times and, therefore, will improve device frequency response.

A series of structures with 100 Å InGaAs base etch-stop layers with InAs mole fractions x between 0.0 and 0.20 indium composition was grown and characterized. Figures 2 through 5 are the Gummel plots for these layers with x = 0.0, 0.10, 0.15, and 0.20, respectively. These figures indicate that the effect of an increase in InAs mole fraction is a reduction in current gain at low collector current densities. This is consistent with the expected increase in recombination center density as the InAs mole fraction at the emitter-base junction is increased with the InGaAs thickness remaining constant. The device with x = 0.20 showed a current gain less than unity for collector currents up to 50 mA. A thinner layer would result in less stress, but InGaAs layers of under 100 Å thickness are not very effective in serving as etch-stop layers.

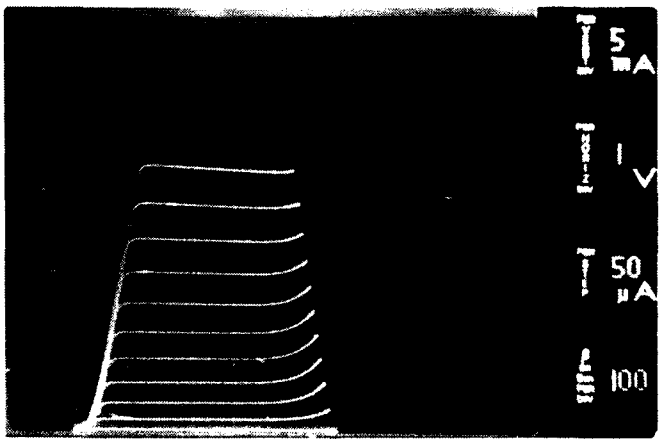


Figure 1
Common Emitter I-V Characteristics of GaAs/AlGaAs HBT With 100-Å-Thick $In_{0.1}Ga_{0.9}As$ Layer in the Base

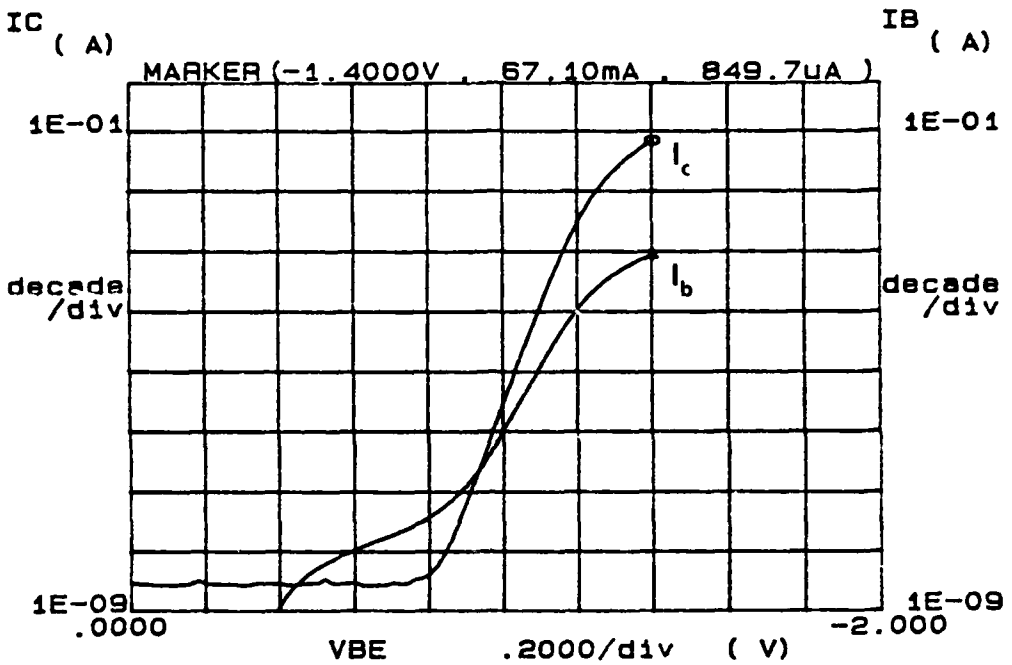


Figure 2

Gummel Plot for GaAs/AlGaAs HBT

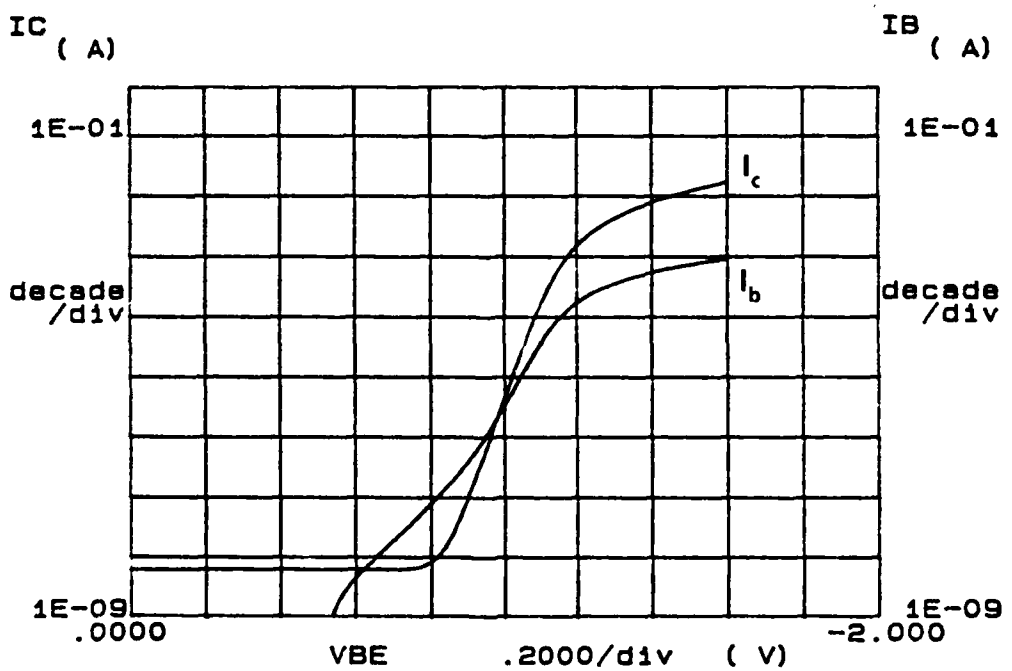


Figure 3

Gummel Plot for AlGaAs/$In_{0.1}Ga_{0.9}As$/GaAs HBT

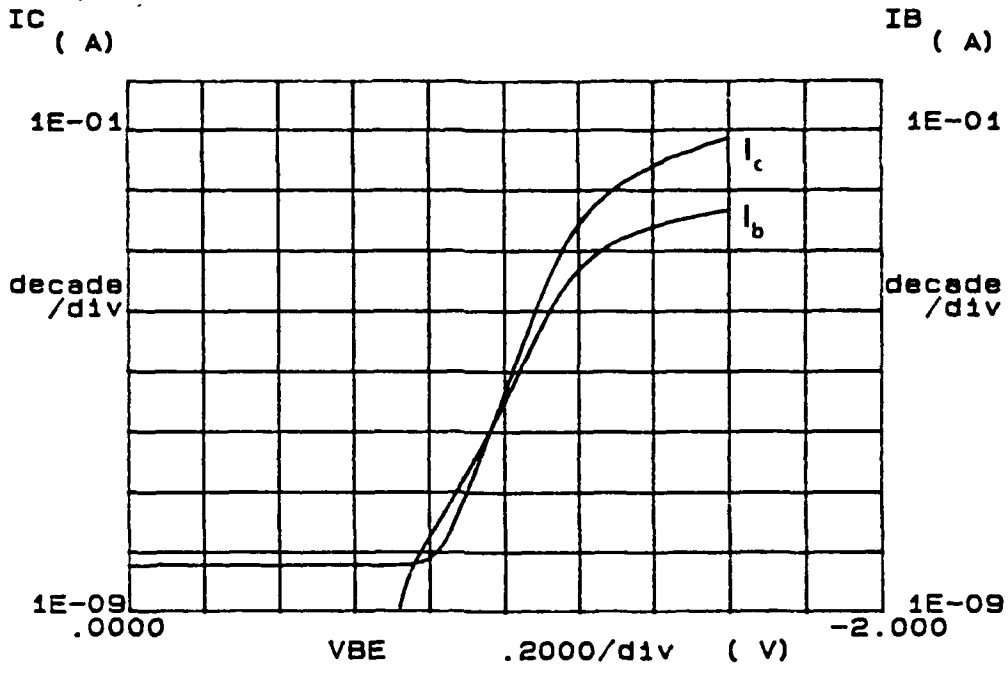


Figure 4

Gummel Plot for AlGaAs/$In_{0.15}Ga_{0.85}As$/GaAs HBT

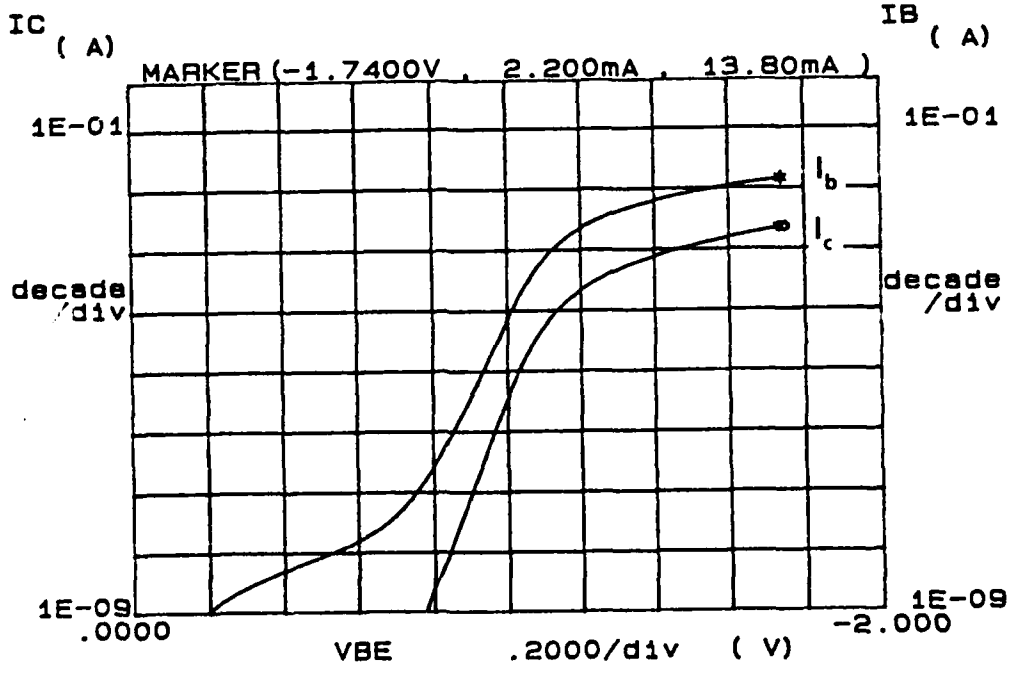


Figure 5

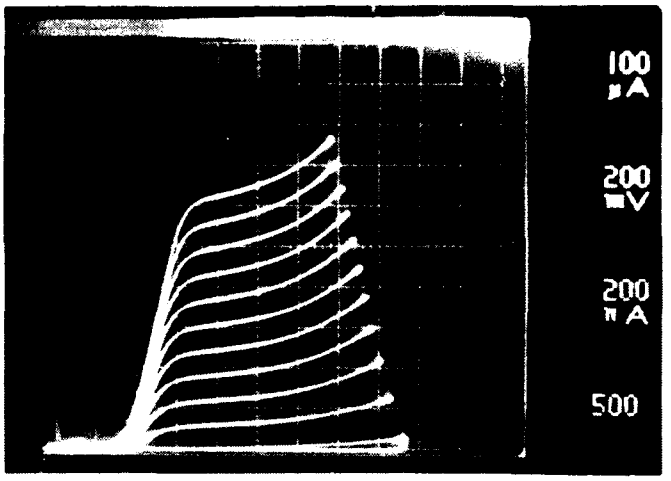
Gummel Plot for AlGaAs/$In_{0.2}Ga_{0.8}As$/GaAs HBT

In accordance with task 1, we are investigating InGaAs/InAlAs HBTs on InP substrates. We have already demonstrated the capability of growing InGaAs/InAlAs structures on 2-inch-diameter InP substrates without the use of indium bonding. This enables us to have a comparatively high throughput of pieces for fabrication.

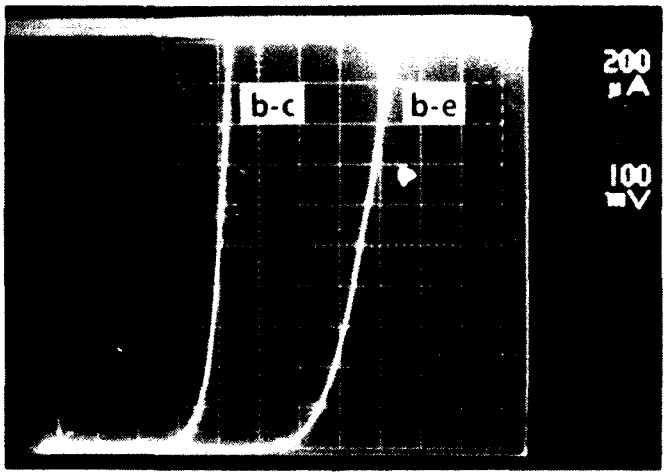
Both single and double heterojunction structures have been investigated. Table 2 shows the layer structure of one of the first SHBT structures that was fabricated under this program. Optimization of the base-emitter junction resulted in very high current gains. Figure 6 shows the common-emitter characteristics for this device. A current gain as high as 1,000 was observed for some devices. Also shown in this figure are the base-collector homojunction and base-emitter heterojunction forward diode characteristics for this device. Both turn-on values are under 1 V; the base-collector turn-on voltage is under 0.5 V, a result of the narrow bandgap of the InGaAs. The large difference in turn-on voltages accounts for the collector-emitter offset that can be observed in the current-voltage characteristics. A Gummel plot for this device is shown in Figure 7 . As can be seen, the current gain is nearly constant over the entire range of current, and there is a very low level of recombination current. The ideality factor for both the base and collector current is 1.3, and the nonideal part of the collector current is probably caused by tunneling of electrons at the emitter-base heterojunction as a result of the large conduction-band discontinuity. Unfortunately, the base-collector reverse breakdown voltage (BV_{cbo}) was only 5 V, 2 V smaller than a similarly structured GaAs/AlGaAs HBT.

Table 2. InGaAs/InAlAs SHBT Structure on InP

Layer	Doping (cm^{-3})	Thickness (μm)
n^+ $In_{0.53}Ga_{0.47}As$	1×10^{19}	0.10
Grading InAlAs→InGaAs	5×10^{18}	0.05
n $In_{0.52}Al_{0.48}As$	2×10^{17}	0.1
Grading InGaAs→InAlAs	2×10^{17}	0.01
n^+ $In_{0.53}Ga_{0.47}As$	1×10^{18}	0.007
p^+ $In_{0.53}Ga_{0.47}As$	1×10^{19}	0.1
n $In_{0.53}Ga_{0.47}As$	3×10^{16}	0.5
n^+ $In_{0.53}Ga_{0.47}As$	5×10^{18}	0.5
Buffer	Undoped	1.0
SI Substrate	Undoped	500 (nom.)



(a) Common Emitter I-V Characteristics



(b) Junction Turn-On Characteristics

Figure 6

InGaAs/InAlAs on InP HBT dc Characteristics With InGaAlAs Transition Layer

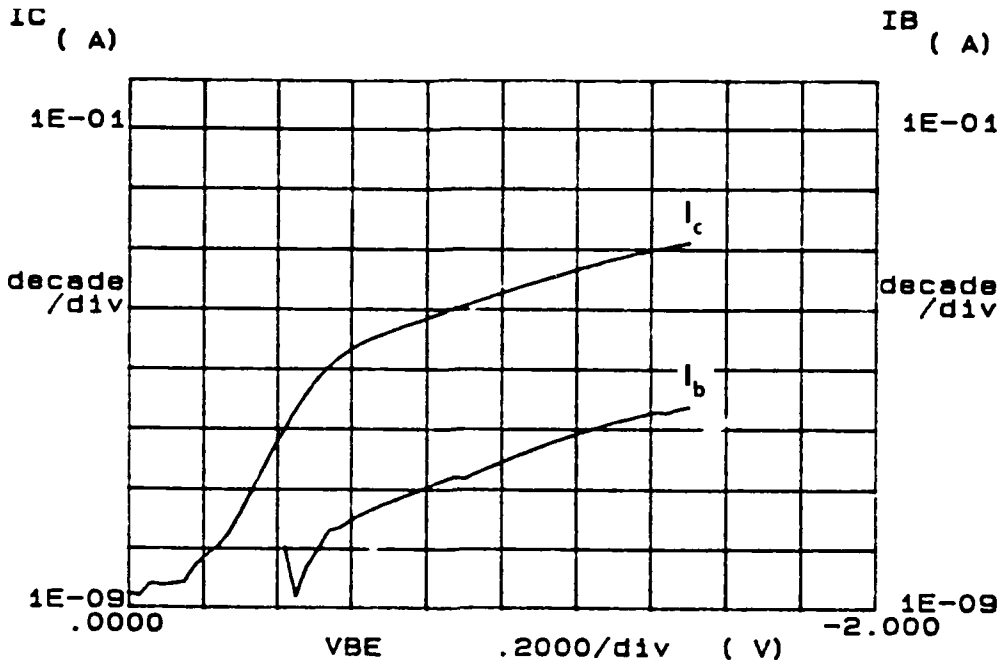


Figure 7
Gummel Plot for InGaAs/InAlAs SHBT on InP

For power applications, a larger value of BV_{cbo} is needed. With this in mind, two SHBT structures shown in Table 3 were grown with 1- and 2-μm-thick collector layers doped 2×10^{16} and 1×10^{16} cm^{-3}, respectively. These layers exhibited large breakdown voltages, the highest we know of for InGaAs/InAlAs SHBTs. The device with the 1-μm-thick collector exhibited a BV_{cbo} of 16 V and a BV_{ceo} of 7.0 V at a collector current of 100 μA for a 9×9 μm^2 device, and a BV_{cbo} of 19 V and a BV_{ceo} of 8.5 V for an 11×11 μm^2 device. A current gain of 15 was observed at a current density of 50 kA/cm^2. The low value of current gain was thought, in part, to result from the high base doping level (1×10^{20} cm^{-3}) for this layer. Figure 8 shows the common emitter characteristics for this device. The layer with the 2-μm-thick collector yielded devices with an even higher BV_{cbo} of 25 V, with a BV_{ceo} of 7.5 V for a 13×13 μm^2 device. This device exhibited poor dc characteristics, however, and had a substantial base-collector reverse-bias leakage current, despite the high breakdown voltage. The latter may account for the BV_{ceo} for this device being only marginally higher than the BV_{ceo} for the first device, despite the significantly higher BV_{cbo} and lower current gain (only 5). It is likely that this structure is so thick that the quality of the epitaxial layer may suffer because of the much longer growth time required. For high-frequency

performance, these structures will exhibit lower collector capacitances but higher collector transit time; a rough calculation predicts that F_t, assuming no delay caused by parasitic resistances and capacitances, would be limited to under 54 GHz and 35 GHz for the 1-μm-thick collector layer and the 2-μm-thick collector layer (both with a 1,000-Å base), respectively. Clearly, neither of these structures will meet the 60- or 94-GHz program goals.

Table 3. InGaAs/InAlAs SHBT Structures With High BV_{cbo} (Collector Thicknesses 1 μm and 2 μm)

Layer	Doping (cm^{-3})	Thickness (μm)
n^+ InGaAs	1×10^{19}	0.20
n^+ InAlGaAs	1×10^{19}	0.05
n^+ InAlAs	1×10^{19}	0.02
n InAlAs	2×10^{17}	0.10
n^+ InGaAs	1×10^{18}	0.01
p^+ InGaAs	1×10^{20}	0.10
n^- InGaAs	2×10^{16} or 1×10^{16}	1.00 or 2.00
n^+ InGaAs	1×10^{19}	0.80
SI InP Substrate	Undoped	625

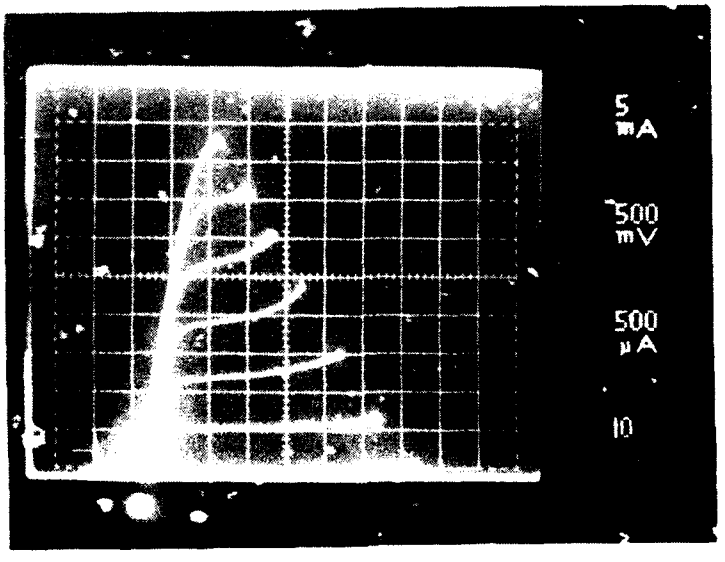


Figure 8

Common Emitter I-V Characteristics of 9×9 μm^2 InGaAs/InAlAs SHBT

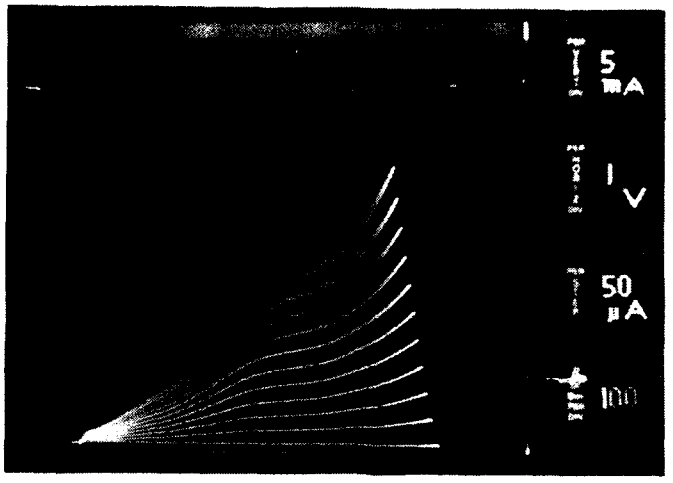
(Collector Thickness = 1 μm, BV_{cbo} = 16 V, BV_{ceo} = 7 V)

In our effort to fabricate a high breakdown voltage InP-based HBT, we have experimented with several InGaAs/InAlAs DHBT structures. Large-area DHBT structures with current gains of 100 and breakdown voltages of 12 to 18 V were fabricated, but these devices also suffered from large offset voltages (several volts) because of a conduction-band spike that blocks electrons at the base-collector interface. This layer had a 60-Å-thick graded layer at the base-collector interface. By introducing a 300-Å graded InGaAlAs n-type spike ($n = 1 \times 10^{18}$), we managed to eliminate the offset voltage, but at the cost of a low BV_{cbo} (5 V at 100 μA), defeating the purpose of the double heterojunction structure. Common emitter characteristics of these two devices are shown in Figures 9(a) and 9(b), respectively.

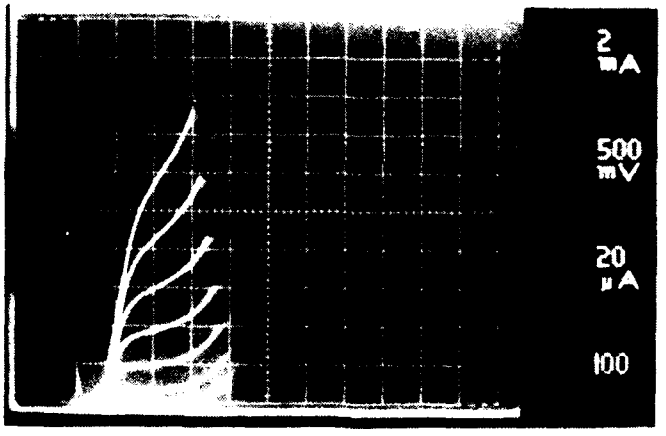
We have also investigated InGaAs/InAlAs structures on GaAs substrates (Task 2). SHBT and DHBT structures were grown by MBE at Texas Instruments on both InP substrates and on lattice-mismatched GaAs substrates with InP buffer layers grown by MOCVD, the latter supplied by Spire Corporation. Figure 10 shows x-ray rocking curve spectra for identical SHBT structures grown on an InP substrate and on a GaAs substrate with an InP buffer layer. All devices exhibited excellent I-V characteristics; Figure 11 shows the common emitter I-V characteristics of an InGaAs/InAlAs SHBT grown on GaAs with an InP buffer layer. Figure 12 shows current gain h_{FE} versus collector current for HBTs with emitter sizes of 11×11 μm^2. At a current of 10 mA (8 kA/cm^2), the DHBT on InP showed a current gain of 300, the DHBT on GaAs a current gain of 100, the SHBT on InP a current gain of 200, and the SHBT on InP a current gain of 80. As can be seen, each device (except the SHBT on InP) exhibits a roughly square-root dependence of current gain on collector current, as is commonly observed in GaAs/AlGaAs HBTs. A Gummel plot of the DHBT on GaAs revealed a high level of leakage current, although this was not observed on the other three devices. The current gain at low collector current levels for the DHBT structures is probably limited because of the difficulty of growing high-quality InGaAs on top of InAlAs; for the HBTs on GaAs, their relatively rough surface morphology, in addition to the propagation of defects through the layers, resulted in a high level of recombination current.

Data on the breakdown voltages BV_{cbo} and BV_{ceo} for these four layers are presented in Table 4. Several trends are clear. First, double heterojunction devices do not show a big improvement in BV_{cbo} despite a higher collector-layer bandgap, which would be expected to reduce avalanche breakdown. This effect was previously noted in this report. BV_{cbo} is clearly higher for the layers on InP than for the layers on GaAs, a result of higher crystal quality and lower defect levels. However, BV_{ceo} is larger for the SHBT on GaAs than for the SHBT on InP, a likely result of the smaller current gain for this device, as:

$$BV_{ceo} = BV_{cbo}/\beta^{1/n}$$

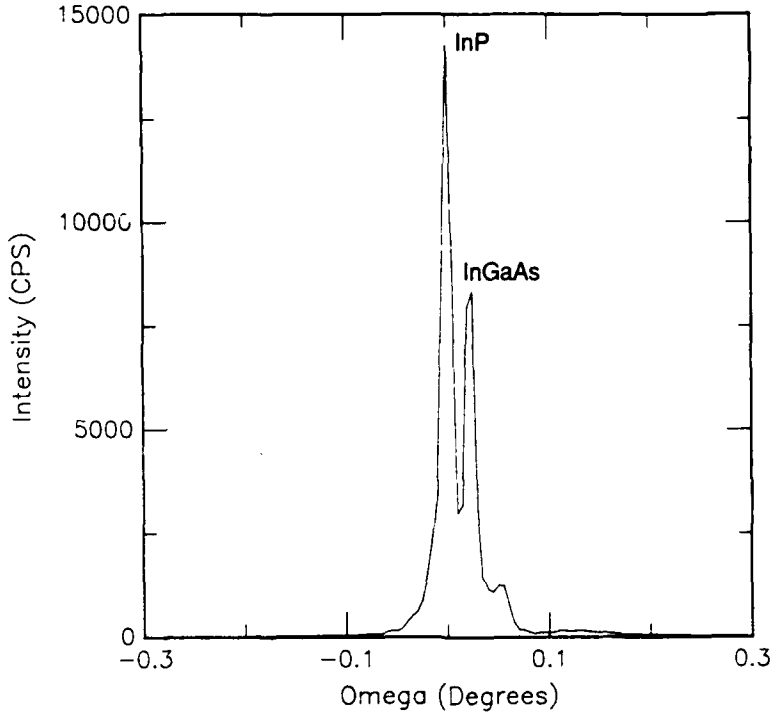


(a) 60 Å Collector-Base Graded Layer

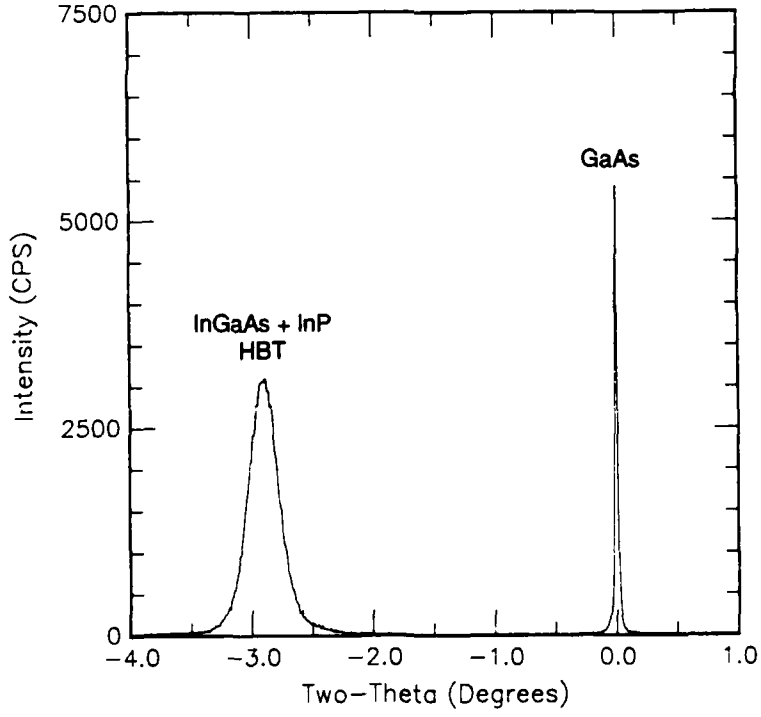


(b) 300 Å Collector-Base Graded Layer With n-Type Spike

Figure 9
InGaAs/InAlAs DHBT Common Emitter I-V Characteristics



(a) On Lattice-Matched InP Substrate



(b) On GaAs Substrate

Figure 10
X-Ray Rocking Curve Spectra for Identical SHBT InGaAs/InAlAs HBT Structures

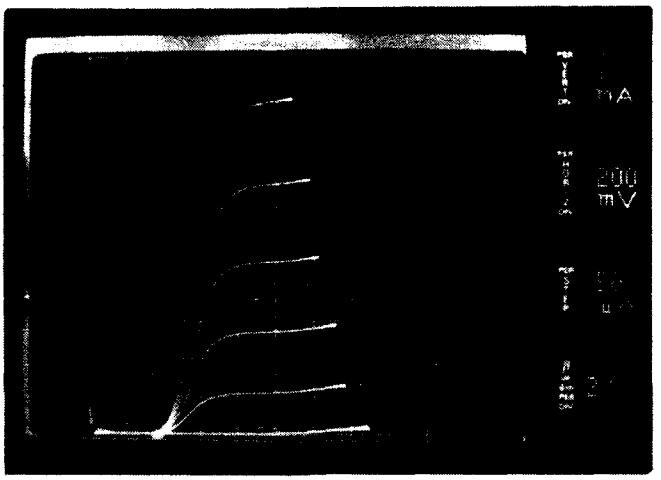


Figure 11

Common Emitter I-V Characteristics of InGaAs/InAlAs SHBT on GaAs
(Emitter Size = $11 \times 11\ \mu m^2$)

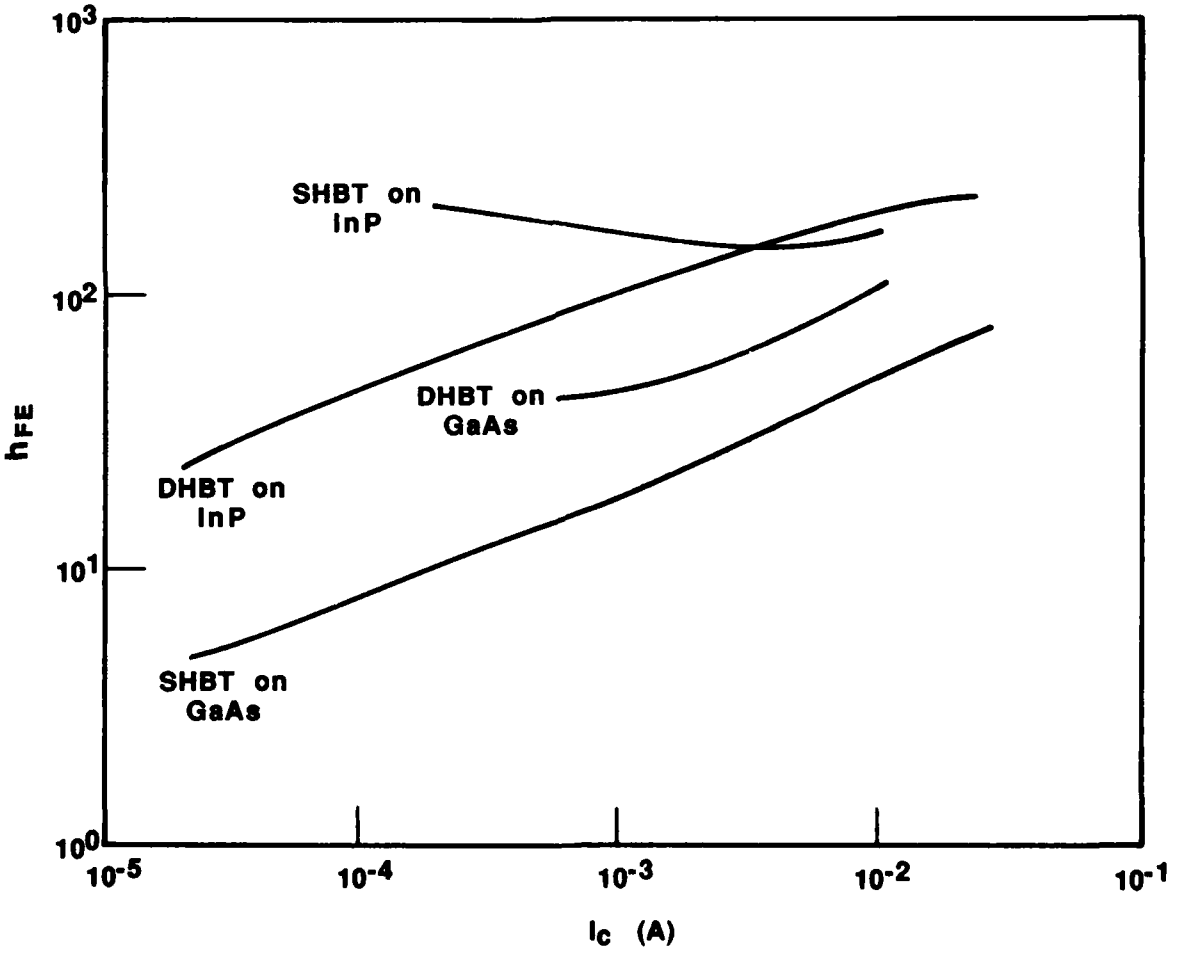


Figure 12

Current Gain h_{FE} Versus Collector Current for InGaAs/InAlAs SHBT and DHBT Structures on GaAs and InP Substrates

Table 4. BV_{cbo} and BV_{ceo} for InGaAs/InAlAs SHBT and DHBT Structures on InP and GaAs

	SHBT on InP	SHBT on GaAs	DHBT on InP	DHBT on GaAs
BV_{cbo} $I_e = 0$, $I_c = 1$ μA	1.1 V	0.8 V	2.5 V	0.3 V
10 μA	2.4 V	2.3 V	3.4 V	0.7 V
100 μA	4.6 V	4.8 V	4.8 V	1.6 V
BV_{ceo} $I_b = 0$, $I_c = 1$ μA	0.9 V	0.7 V	1.3 V	0.5 V
10 μA	1.1 V	1.5 V	1.6 V	0.8 V
100 μA	1.7 V	2.9 V	1.9 V	1.3 V

While the HBTs on InP exhibited superior dc performance to the HBTs on GaAs, the performance of the HBTs on GaAs with InP buffers merits further study.

An SHBT structure on GaAs was also grown with an $In_{0.53}Ga_{0.47}As$ buffer layer that has an otherwise identical structure to those grown with an InP buffer layer. Unfortunately, this SHBT structure had a poor surface morphology, much worse than had been noticed on the InP buffer structures, and the current gain was limited to 10, with a high level of leakage current and low diode breakdown voltages. This reaffirms our opinion that InP is the most suitable material for a buffer layer for indium-based compounds on GaAs.

In addition to npn structures, we have also investigated pnp structures (Task 7). A large-area GaAs/AlGaAs pnp showed a current gain of 100 at a current density of 400 A/cm^2. In addition, the breakdown voltage for this structure, shown in Table 5, was 20 V. We have also designed an InGaAs/InAlAs pnp HBT structure which we expect to receive in early 1990, shown in Table 6.

Table 5. Vertical Structure of GaAs/AlGaAs pnp SHBT

Layer	Doping (cm^{-3})	Thickness (μm)
p^+ GaAs	1×10^{19}	0.10
p Grading	1×10^{18}	0.03
p $Al_{0.3}Ga_{0.7}As$	2×10^{17}	0.05
n^+ GaAs	1×10^{18}	0.09
p GaAs	2×10^{16}	1.0
p^+ GaAs	1×10^{19}	1.5
AlGaAs Buffer	Undoped	0.3
SI Substrate	Undoped	625

Table 6. Structure of InGaAs/InAlAs pnp SHBT

Layer	Doping (cm^{-3})	Thickness (μm)
p^+ InGaAs	1×10^{19}	0.20
p^+ InGaAlAs	1×10^{19}	0.05
p^+ InAlAs	1×10^{19}	0.02
p InAlAs	2×10^{17}	0.10
n^+ InGaAs	1×10^{19}	0.10
p^- InGaAs	3×10^{16}	0.70
p^+ InGaAs	1×10^{19}	0.80
SI InP Substrate	Undoped	625

Finally, we have designed and received a new mask set to be used specifically for InGaAs/InAlAs HBTs on GaAs substrates. Figure 13 shows the design of a self-aligned HBT with a 4×4 μm^2 emitter. Table 7 summarizes the dimensions of the different transistor structures that will be investigated with this mask set. The T1X and T3X series are similar, as are the T2X and T4X series. The transistor shown in Figure 13 is T1D. The mask set has seven levels, and the process flow is as follows. First, the emitter ohmic metal is evaporated and lifted off. Then, dry etching is used to reach the base mesa. Following this, nitride sidewalls are formed, and the base metal is evaporated, self-aligned to the emitter. After that, a collector etch is performed, and the collector metal is deposited into the etched portion defined by the collector etch. An isolation (wet) etch is performed, and gold is deposited on the patterned substrate to form contact pads. Then, a dielectric layer is deposited on the entire substrate, vias are etched in the dielectric, and gold plating connects the ohmic metals with the probe pads.

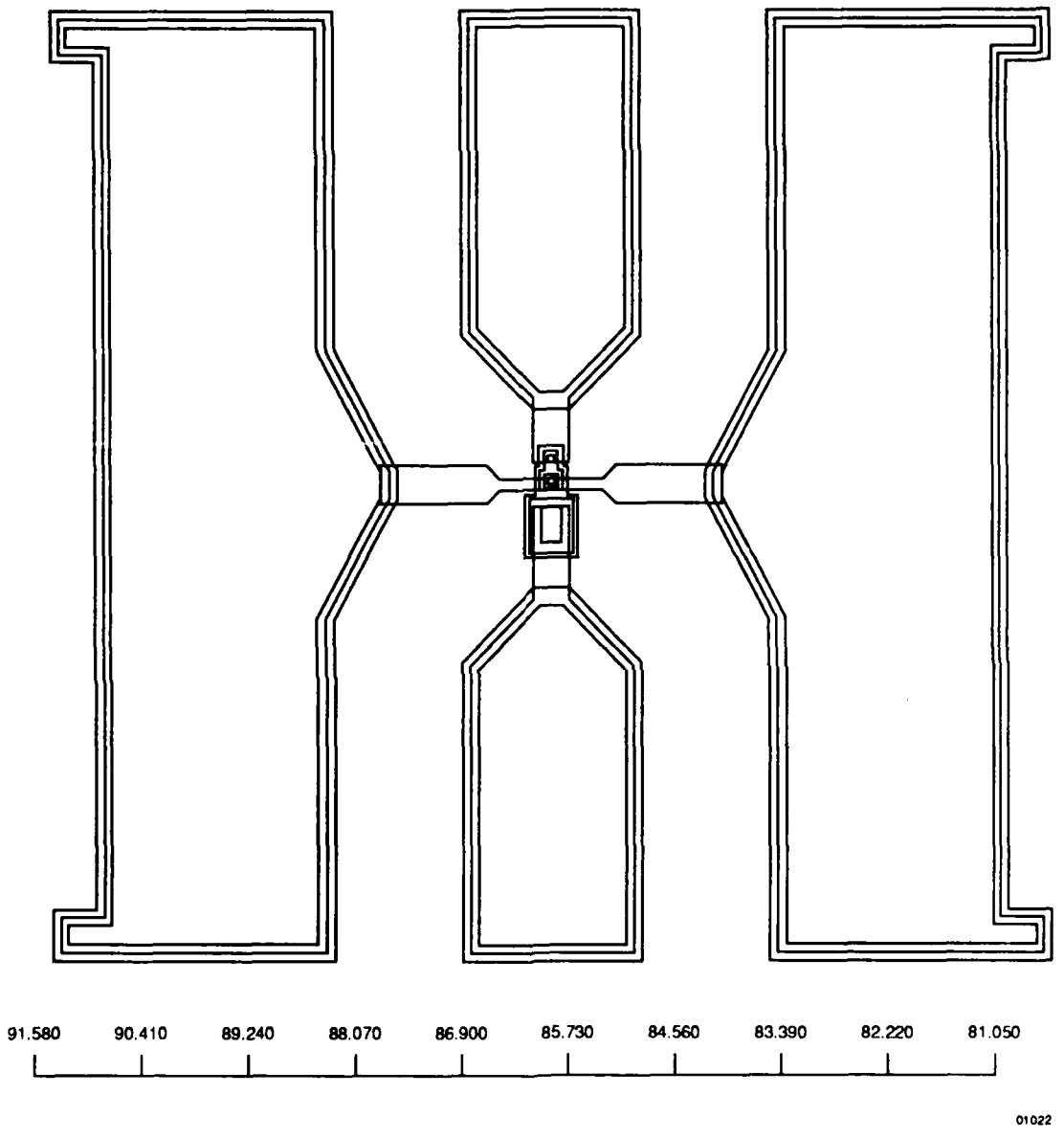


Figure 13
Self-Aligned HBT With 4×4 μm^2 Emitter

Table 7. Transistor Dimensions for New Mask Set

Position	Emitter	Base Mesa	Isolation Mesa	Emitter Vias
T1A	5 × 5	13 × (7,5)	31 × (12,10,8)	3 × 3
T1B	5 × 5	12 × (7,4)	30 × (12,10,7)	3 × 3
T1C	4 × 4	12 × (6,5)	30 × (12,9,8)	2 × 2
T1D	4 × 4	11 × (6,4)	29 × (12,9,7)	2 × 2
T1E	4 × 4	11 × (6,4)	29 × (12,9,7)	2 × 2
T2A	10 × (4,2)	16 × (6,4)	(34,33) × 13	2 × 2
T2B	15 × (4,2)	21 × (6,4)	(39,38) × 13	2 × 2
T2C	10 × (3,2)	16 × (5,4)	(34,33) × 12	2 × 2
T2D	15 × (3,2)	21 × (5,4)	(39,38) × 12	2 × 2
T2E	10 × (3,2)	16 × (5,4)	(34,33) × 12	2 × 2
T3A	5 × 5	13.5 × (7,5)	32 × (12,10,8)	3 × 3
T3B	5 × 5	12.5 × (7,4)	31 × (12,10,7)	3 × 3
T3C	4 × 4	12.5 × (6,5)	31 × (12,9,8)	2 × 2
T3D	4 × 4	11.5 × (6,4)	30 × (12,9,7)	2 × 2
T3E	4 × 4	11.5 × (6,4)	30× (12,9,7)	2 × 2
T4A	10 × (4,2)	16 × (7,5)	(35,34) × 15	2 × 2
T4B	15 × (4,2)	21 × (7,5)	(40,39) × 15	2 × 2
T4C	10 × (3,2)	16 × (6,5)	(35,34) × 14	2 × 2
T4D	15 × (3,2)	21 × (6,5)	(40,39) × 14	2 × 2
T4E	10 × (3,2)	16 × (6,5)	(35,34) × 14	2 × 2

Note: More than one length or width in a given dimension is indicated by parentheses ( ).

III. FUTURE PLANS

In the next year, we plan to fully develop our self-aligned HBT fabrication procedure, optimizing our dry-etch process with a Plasma Quest ECR reactor. We also intend to develop a method to fabricate small geometry structures with a suitable isolation technique for reducing parasitic device capacitance. Also, we expect to start the millimeter-wave measurement and characterization of InGaAs/InAlAs HBTs, and develop a large-signal device model of the HBT.

We will also study the tradeoffs involved in collector design for SHBT layers. Collector doping and thickness are the key parameters for this program, as it is likely that collector transit time will limit high-frequency performance, and base-collector breakdown will limit power output. For the 5×5 μm emitter structure on our mask set (device T1B), for instance, with an 800-Å base layer doped 1×10^{20} cm^{-3}, an emitter doped 1×10^{18} cm^{-3}, and a 1-μm-thick collector doped 2×10^{16}, we estimate an F_t of 52 GHz, and a BV_{cbo} of 19 V. For a similar structure with a 4,000-Å-thick collector, we estimate an F_t of 77 GHz and a BV_{cbo} of 8 V; BV_{ceo} will be even smaller. For the same structure, it would take a collector thickness of 2,000 Å (and an associated BV_{cbo} of 3 V) to obtain an F_t of 94 GHz. The immediate objective for the year is to fabricate an HBT with an output power of 1 W at a frequency of 44 GHz, with a gain of 6 dB and an efficiency of 40 percent. We intend to achieve this with an InGaAs/InAlAs SHBT structure on GaAs.

In accordance with the program tasks, we also intend to fabricate, test, and model pnp InGaAs/InAlAs structures, both on InP and GaAs, as well as both npn and pnp InGaAs/InP SHBT and DHBT structures grown by MOCVD and gas-source MBE.